Abstract Submission

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Thank you **Satish Bonam** for submitting your abstract to the 65th ECTC. You will be notified of the results of the program selection committee by December 14, 2014. Please contact me for further assistance.

Sincerely,

Henning Braunisch
65th ECTC Program Chair

The abstract and information you submitted appears below:

Password	04c01a0485
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Location

Sheraton San Diego Hotel & Marina
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Add a note here for selecting two different committees.

Primary Subcommittee:

Advanced Packaging

Secondary Subcommittee:

Interconnections

Keyword 1:
3D integration

Keyword 2:
TSV

Keyword 3:
interconnect processes

Keyword 4:
substrates

Keyword 5:
reliability

Keyword 6:
None

Student Awards:

IEEE Travel Award

Abstract:

Three dimensional integration circuits (3D IC) with Through silicon via (TSV) technology is the most important technology for scaling down IC dimensions as it reduces the path length, increases I/O lines density thereby increasing speed with minimal power consumption. TSV creation requires relatively high etch rate, anisotropic etch independent of crystal orientation and relatively high smoothness on side walls. These processes are typically costly and requires sophisticated high end equipment like Deep Reactive Ion Etching. In this work an alternative, low cost, robust method of making TSVs is proposed and validated. This method is inspired from Metal assisted chemical etching (MACE) process that is regularly used to produce porous silicon and vertically aligned semiconductor nanowires. The primary advantage of this process is that it is a very simple, well understood wet chemical process devoid of the usage of high end equipment. In MACE process, the material whose nanowires have to be formed is taken as substrate and nanowires are formed using a simple metal assisted catalytic etching process. However complete through etching of the substrate has not been performed and the structure morphology has not been studied or reported. The value addition of such study pertaining to silicon as substrate is enormous as they etched portions can potentially form TSVs. A controlled, vertically aligned TSV through this problem is a solution to one of the major bottlenecks that 3D IC technology is facing which is to achieve highly reliable, repeatable TSVs. This method contains two steps. First, a lithographically patterned noble metal film (Ag, Au, Pt, Pd) is deposited onto silicon substrate. Second, the etching of the silicon is carried out in a solution containing HF and oxidative agent (H_2O_2). In MACE, holes are generated through redox reactions at the interface of the metal film and the Solution. The metal layer acts as a catalyst for the reduction of oxidative agent. The generated holes are injected into the Silicon substrate directly beneath the metal film and then gets oxidized . The oxidized silicon beneath the metal gets dissolved by the HF leaving the metal in its original form. Consequently the metal film sinks into the formed via. This process can be continued till the desired depth or through hole in Si is achieved. In this work, we report the fabrication of array of circular TSVs having a diameter of 40 micrometer separated by a pitch of 60 micrometer on a (100) P-type silicon wafer (Resistivity: 1- 10 ohm-cm). Gold was used as a catalyst and an ultrathin layer of the same is sputtered on the array which is formed using S1813 positive photoresist. TSV formation was carried out in HF and H_2O_2 etchant. Successful formation of TSVs

was observed. Encouraged by these results, the further characterization and optimization of fine pitch, high aspect ratio TSV is being carried out. .

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